REMARKS/ARGUMENTS

In the Office Action, claims 41 and 44 have been rejected under 35 U.S.C. 102(b) as being anticipated by United States Patent 5,781,549 to Dai.

With reference first to the rejected independent claim 41, this claim recites an integrated circuit having one or more active output ports and comprising a memory manager that stores chunks of information into buffers in a payload memory. All of the buffers are of equal size. Some of the chunks of information include cell information, and others of the chunks of information include packet information. The integrated circuit also comprises reassembly means for receiving the chunks from the memory manager and for performing one reassembly process per active output port such that substantially no more than one reassembly context is maintained for each active output port.

According to page 2 of the Office Action, Dai discloses a network device 100 having one or more ports and comprising a packet processing unit 200 for storing information into a memory 210 with buffers of equal side. The Office Action proceeds to state that the packet processing unit 200 includes a reassembly means 700 for receiving information from the memory 210 and for performing one reassembly process per port such that no more than one reassembly context is maintained for each port.

Regarding the claimed feature of performing one reassembly process per active port, as recited in rejected independent claim 41, the Office Action refers to Figure 7 and column 10, lines 29 to 35 of Dai, and notes that the linked list control logic 750 maintains one packet transmission line per port. With respect, Applicant notes that packet assembly is not performed in the packet transmission lines of Dai, but rather in packet assembly lines.

With reference to column 9, lines 42 to 46, Dai discloses that the packet assembly linked list control logic 730 comprises 25 packet assembly lines for 24 ten Mbps low speed packet data flow packets and a single high-speed packet data flow, respectively. Dai proceeds at line 46 of column 9 to describe operations performed when a cell is received from the cell bus 220, and in particular indicates that the appropriate packet assembly line for a received cell is found based on source information in the cell header, and the packet assembly line is directed to perform

assembly operations.

The portion of column 10 referenced in the Office Action introduces packet transmission lines. As noted in the Office Action, the packet transmit linked list control logic 750 maintains 8 packet transmission lines for each of 8 local ports respectively associated with the packet processing unit 200. Although only 8 local ports are associated with a packet processing unit 200 in Dai, 25 packet assembly lines are maintained in that same packet processing unit. Clearly, the packet processing unit 200 of Dai does not restrict reassembly operations to one reassembly process per port.

This is further evidenced, for example, at lines 48 to 56 of column 11, at which Dai discusses a scenario in which assembly of another packet destined at a port is completed while a current packet transmission is still in process. In this case, the new completed packet will be attached "to the back of the packet transmission line".

Thus, in Dai, packets may be assembled in multiple packet assembly lines, at the same time, for the same port. Dai discloses that a packet processing unit maintains 25 packet assembly lines but only 8 ports, and that multiple packets may be destined for the same output port. The 8 packet transmission lines in Dai are not involved in the packet assembly process, and accordingly the provision of one packet transmission line per port does not provide the claimed feature of performing one reassembly process per active port, as recited in rejected independent claim 41.

Claim 41 also recites that substantially no more than one reassembly context is maintained for each active output port. The Office Action refers to Figure 8, lines 57 to 67 of column 10, and a packet attribute 820 as allegedly disclosing this feature. However, there is no disclosure in Dai that would suggest a function or effect of the packet attribute 820 as limiting the assembly process performed in the packet assembly lines to one process per port.

Dai fails to disclose all of the limitations recited in independent claim 41. It is thus respectfully submitted that independent claim 41, as well as rejected claim 44 which depends therefrom, are allowable over Dai, and that the anticipation rejection under 35 U.S.C. 102(b) should be reconsidered and withdrawn.

Applicant thanks the Examiner for acknowledging that claims 20 to 22, 34 to 40, 42, and 43 include allowable subject matter. Applicant wishes to note, however, that the statement of reasons on page 3 of the Office Action reflect the Examiner's characterization of the claimed subject matter. Other interpretations of the allowed claims are possible.

In view of the foregoing, Applicant respectfully submits that all of the claims 20 to 22 and 34 to 44 are allowable, and early action to this end is earnestly solicited.

Respectfully submitted,
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